Taking Back the Power: Power Design Techniques for your Next SoC

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ABSTRACT

Any power network has voltage losses and current demands. Designers must limit the losses while meeting the demands in order for a device, circuit and system to function properly and within its specifications. Whether your design targets automotive, IoT, or infrastructure; understanding how to optimally design your SoC power can lead to substantially different results, whether you want fast performance or low power. The complex topic of power distribution and design is more complex than ever with the move to FinFET processes. The double patterning forces strict design rules, which in turn limit the available, optimal power grids. Without knowledge of the detailed design rules and the chosen architecture for a given library, designers can be left with sub-optimal designs due to their selected power grid.

This paper outlines generally recommended practices, based on power distribution experience and cell library architecture. Topics covered include the main goals and considerations in supply distribution, what structural changes might be expected in different market segments, and the stringent requirements of double-patterned processes.

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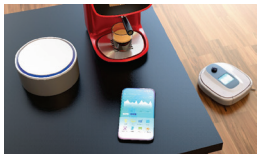
Different markets will optimize power grids differently

Mobile Market

- Faster and richer user experience
- Higher frequency
- Low-power and leakage

IoT Market



- Longer batter life
- Lower frequency
- Lower power and leakage

Automotive Market

- Self driving car
- Longer battery life
- Higher or lower frequency depending on application

PPA targets impact a power grid

and a power grid can impact PPA

Specification	Mobile	IoT	Automotive	
Core	Cortex®-A73	Cortex®-M33	Cortex®-A*	Cortex®-M*
Process	TSMC 12FFC/ 16FFC	TSMC 40ULP	TSMC 16FFC auto	TSMC 16FFC auto
Frequency	3GHz	50MHz	> 1GHz	< 1GHz
Dynamic Power	<200mW/GHz/CPU	>10uW/MHz	Can support higher power	Lower power
Leakage	< 70mW	< 6.75uW	Can support higher leakage	Lower leakage

Power requirement varies from 200mW to 10uW for different market segments

Power planning is key

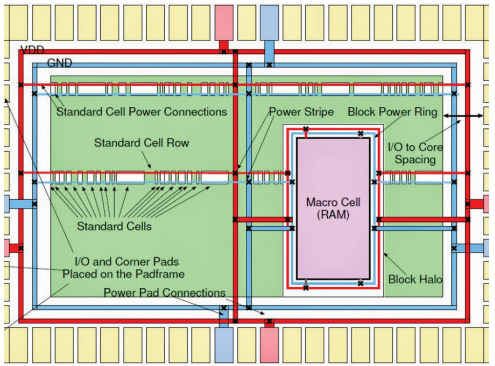
Power planning is a step where power grid network is created to distribute equal power to each part of the design

Proper Power Grid helps to achieve

- Smaller IR drop
- Very high speed design possibility

This step involves placement of

- Core power ring
- Standard cells power hook up
- IO/ Block power hook up



Power distribution

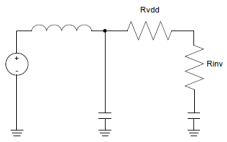
Power distribution methods should assist in mitigating the effects of on-chip resistance and inductance while taking advantage of the cell architecture to maximize density

There are two main goals in supply distribution and design

1. Get the target voltage supply level as close to the transistors as possible
2. Block the least amount of routing resources

To get the target voltage supply level as close to the transistors as possible, you must:

- Control the IR drop
- Control the di/dt response



Simple RLC power network

Good supply distribution mitigates the effects of on-chip resistance and inductance

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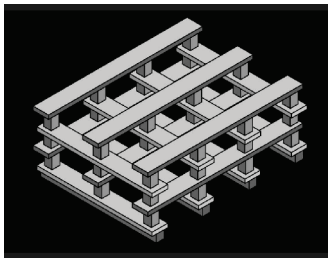
Three parts of the power grid

The support structure for the entire design

1. Structures to support static IR drop based on the peak power density
   - Limited frequency response due to impedance between the power regulator and the standard cells
2. Structures to support fast transient response to dynamic IR
   - Requires a low impedance path to nearby capacitance, either inherent to the design or from decap
3. Power gating switches and enabling the power gating switches
   - Optional



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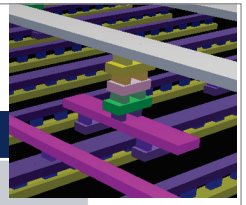
Power supply overview



Standard Cell design (Arm®)	Chip/block design (customer)	Reason
Largest cell supply rail possible		• Reduces IR drop • Improves EM characteristics • Allows for greater redundancy of supply vias (IR, EM, yield)

	Lower 2D supply grid (M2/M3)	• Reduces di/dt
		• Reduces resistance
		• Reduces on-chip inductance to local decoupling capacitance
		• Reduces VIA resistance versus using only an upper supply grid
		  • Current doesn't need to travel up the stack and back down
		  • Smaller impedance induced supply droop (avoids large delay degradations)

	Upper 2D supply grid (top 2 metals)	• Reduces IR drop • Handles global supply distribution • Improves routing by freeing lower planes for signal routing
	Both grids	• Narrow straps placed frequently • Evenly spaced • Power and ground on all layers • Power and ground straps alternate

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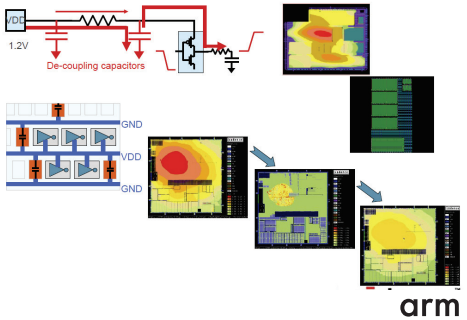
The IR drop challenge

A robust power-aware design methodology should include:

- Up-front, preventive steps
  - Automatic or assisted power planning (placement, routing+ de cap insertion)
- Optimization steps
  - De-coupling capacitance size and location
- Sign-off
  - Understand IR drop impact on timing and SI noise

The IR drop challenge

Static and dynamic analysis



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Decoupling capacitors

Decap cells are important in every design

- Keeps the charge close to the transistors
- Enables fastest switching and limits di/dt

IoT SoCs need to go beyond standard cell decoupling capacitors – to manage current draw from active duty cycles (wake up)

Need to placed around the boundary of the chip and radio to prevent noise on the power lines and interference with the radio circuitry

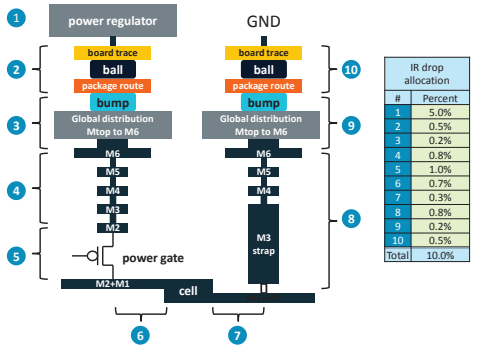
IR drop sources and example budgets

Total budget is 5% or 10%

- For static plus a weighted average dynamic IR drop
- Aligns with the voltages in the worst case PVT corners
- 10% shown here

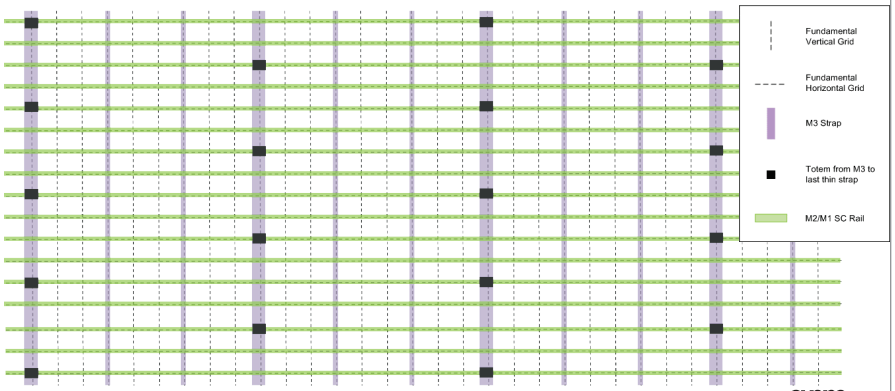
Adjust as needed for each design

Note the recommended IR drop across power gates is 1% (#5)

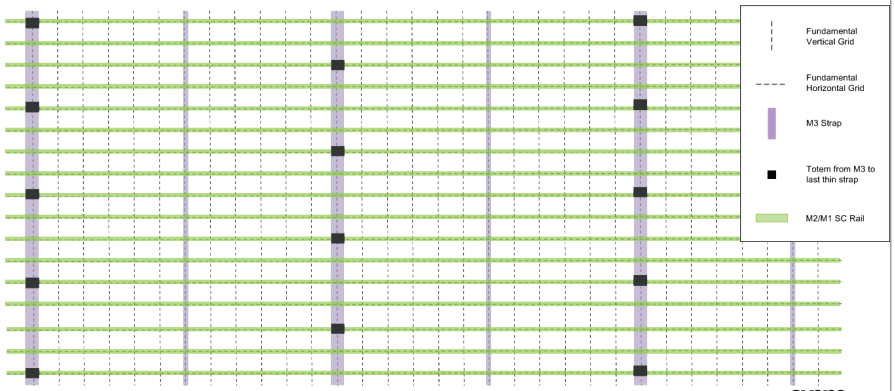


IR drop allocation	
#	Percent
1	5.0%
2	0.5%
3	0.2%
4	0.8%
5	1.0%
6	0.7%
7	0.3%
8	0.8%
9	0.2%
10	0.5%
Total	10.0%

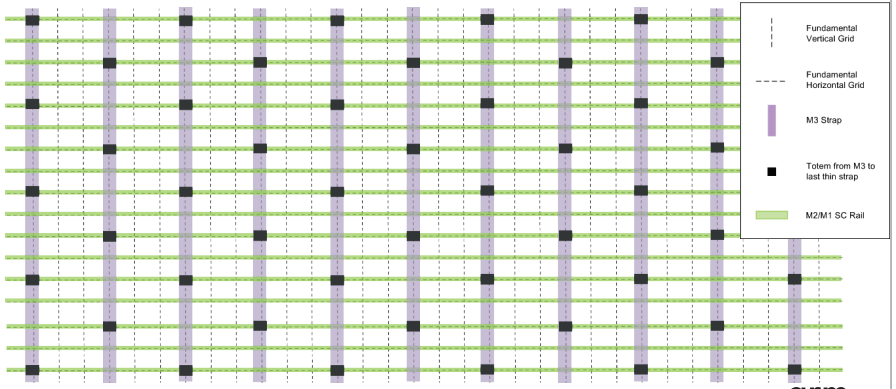
Example lower 2D power grid



Lower grid for low-power density designs



Lower grid for higher power density designs



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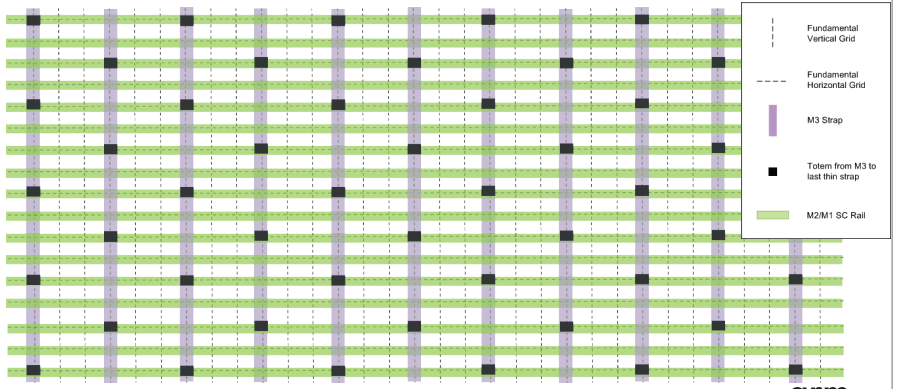
Lower grid for extreme power density designs



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Impact of double patterning

Traditional power grids used M1

- Maybe a 2D lower grid on M3 or M5

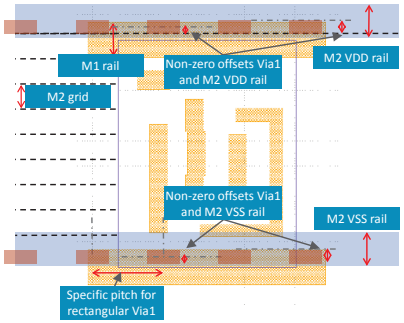
Standard cell power rails were centered at the cell boundary

Standard VIAs were used

- Double VIAs followed

Strict and complex double patterning and cell architecture selection changes the tradition

- Limits available options
- More complex to implement



16nm example, 2 track M2 rail option

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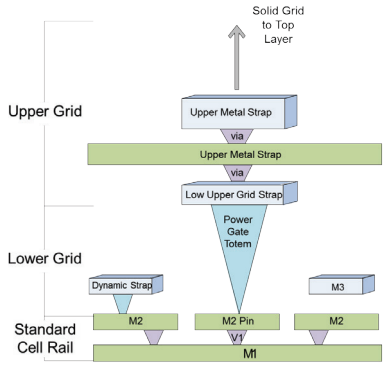
Arm Artisan Power Grid Architect

Arm® Power Grid Architect (PGA) automates critical aspects of floorplanning

- Extremely critical for FinFET and double pattern designs
- Useful for complex power grids in 28nm
- PGA runs on industry-standard floor planning tools

PGA can create power grids which can support different markets

- Technology specific routing files are provided with PGA utility
- Designers can be left with sub-optimal designs with their selected power grid for any cell architecture



Illustrated power network with power gating

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Power Grid Architect Features

PGA supported features

- Basic standard cell grid insertion
- Post route via insertion
- Power switch (header type) insertion and connection to power grid
- Floorplan checking
- Boundary cell insertion
- Connect memories to the grid
- Sleep signal stitching
- Multiple power domains
- Healing of power switches and straps when interrupted by hard macros
- Secondary supply regions

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Summary

A power grid is critical

- Different markets will optimize power grids differently

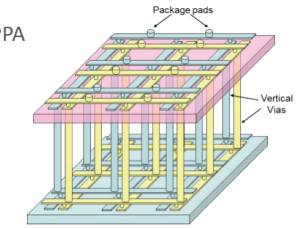
PPA targets impact a power grid, and a power grid impacts PPA

Supporting complex design power distribution

- Optimal power distribution is key to achieve lowest and uniform IR drop
- Appropriate power grid can help to achieve optimal power distribution

Strict and complex double patterning and cell architecture selection changes the tradition

- Limits available options
- More complex to implement



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